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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ZIMMERMAN, GLENN	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,718	TAKENAKA ET AL.	
	Examiner	Art Unit	
	Glenn Zimmerman	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment, filed on December 10, 2004, has been entered and acknowledged by the examiner.

Allowable Subject Matter

The indicated allowability of claims 4-7 are withdrawn in view of the newly discovered reference(s) to Ge et al. U.S. Patent Application Publication 2002/0000771A1 and Ge et al. U.S. Patent 5,859,508. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the first spacers" in claim 10. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the first spacer" in claim 11. There is insufficient antecedent basis for this limitation in the claim.

A 112 2nd paragraph rejection has been determined for claim 1, as written about above. However, a further evaluation of the claim will be done while interpreting "the first spacers" in line 10 as "the spacers".

A 112 2nd paragraph rejection has been determined for claim 1, as written about above. However, a further evaluation of the claim will be done while interpreting "the first spacer" in line 11 as "the spacers".

Claims 2-9 are rejected for depending from a rejected base claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415 and Hisafumi Japanese Patent Application Publication 07-326306.

Regarding claim 1, Ge et al. teaches an image display device **(title)** comprising: a first substrate **(Fig. 1 anode plate ref. 12)** including an image display surface **(ref. 52 viewing direction)** and a metal back **(ref. 32 Al coating)** formed on the image display surface a second substrate **(cathode substrate ref. 16)** opposed to the first substrate across a gap **(Fig. 1 no ref. #)** and including a plurality of electron sources **(FE cathodes ref. 14, 14g, 14b, 14r)** which excite **(dotted lines Fig. 1)** the image display surface; a grid **(electrically conductive layer ref. 50)** provided between the first and second substrates and including a plurality of beam passage apertures **(through hole Fig. 1)** opposed to the electron sources, individually; a plurality of spacers **(anode spacer ref. 60 along with cathode spacer ref. 56)** which maintain the space between the first substrate and the second substrate; and a voltage supply unit **(power supply in controller ref. 44)**, but fails to teach the voltage supply unit applies a first voltage to the first substrate and applies a second voltage higher than the first voltage to the grid. Compain et al. in the analogous art teaches A voltage supply unit which applies a voltage to the anode and applies a voltage higher than the one for the anode to the grid **(Fig. 5)**. Additionally, Compain teaches incorporation of such a higher voltage to improve the forbidding of generated parasitic ions from reaching the cathode or the anode **(abstract; Fig. 5)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a voltage supply unit which applies a voltage to the first substrate and applies a voltage to the first substrate and applies a voltage higher than the one for the first substrate to the grid in the image display of

Takenaka, since such a modification would improve the forbidding of generated parasitic ions from reaching the cathode or the anode as taught by Compain.

Regarding claim 1, Ge et al. and Compain et al. teach all of the limitations of claim 1, but fail to teach a height correcting layer interposed between each of the spacers and the first substrate and abutting against the spacers and the first substrate;. Hisafumi in the analogous art teaches a height **(Drawing 3 ref. 15 elastic body)** correcting layer interposed between each of the first spacers **(ref. 14)** and the first substrate **(ref. 11)** and abutting against the first spacer and the first substrate. Additionally, Hisafumi et al. teach incorporation of such a height correcting layer to improve the product since the tensile stress value which acts on the front plate, front face and back plate is decreased by 10% and improved breakage prevention is attained **(paragraph 39)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a height correcting layer interposed between each of the first spacers and the first substrate and abutting against the first spacer and the first substrate in the spacer of Ge et al. and Compain et al., since such a modification would improve the product since the tensile stress value which acts on the front plate, front face and back plate is decreased by 10% and improved breakage prevention is attained as taught by Hisafumi et al.

Regarding claim 2, Ge et al. disclose an image display device according to claim 1, wherein the grid includes a first surface opposed to the first substrate and a second surface opposed to the second substrate **(See Fig. 1)**; and the spacers include a

plurality of columnar **(Fig. 3A, 3B)** first spacers **(anode spacer ref. 60)** set up on the first surface of the grid and abutting against the first substrate and a plurality of columnar **(Fig. 3A, 3B)** second spacers set up on the second surface **(cathode spacers ref. 56)** of the grid and abutting **(Fig. 1 no ref. #)** against the second substrate.

Regarding claim 3, Ge et al. disclose an image display device according to claim 2, wherein each of the first spacers is set up on the first surface of the grid between the beam passage apertures **(See Fig. 1 dotted lines and anode spacer ref. 60)**, and each of the second spacers is set up on the second surface of the grid between **(See Fig. 1 dotted lines and cathode spacer ref. 56)** the beam passage apertures and aligned **(Fig 1)** with the first spacer.

Regarding claim 4, Ge et al. disclose an image display device according to claim 2, wherein the first spacers are shorter **(paragraph 19)** than the second spacers in height **(paragraph 19)**. The examiner notes that the cathode spacer is **about** 10 to 500 microns. Therefore then choose 510 microns or 501 microns which is 0.51 or 0.501 mm which is about 500 microns. The examiner notes that the anode spacer is about 0.5 mm. Therefore the cathode spacer (second spacer) can be chosen to have greater height than the anode spacer (first spacer).

Regarding claim 9, Compain et al. discloses an image display device according to claim 1, wherein the second voltage applied to the grid is set less than or equal to 1.5 times as high as the first voltage applied to the first substrate **(abstract; Fig. 5)**. This claim is rejected for the same reasons found in claim 1.

Regarding claim 10, Ge et al. teaches an image display **(title)** device comprising a first substrate **(Fig. 1 anode plate ref. 12)** including an image display surface **(ref. 52 viewing direction)** and a metal back **(ref. 32 Al coating)** formed on the image display surface; a second substrate **(cathode substrate ref. 16)** opposed to the first substrate across a gap **(Fig. 1 no ref. #)** and including a plurality of electron sources **(ref. 14)** which excite the image display surface **(RGB ref. 33)**; a grid **(ref. 50)** provided between the first and second substrates and including a first surface opposed to the first substrate, a second surface opposed to the second substrate and a plurality of beam passage apertures **(through hole no ref. #)** opposed to the electron sources, individually; a plurality of spacers **(ref. 60 and 56)** including a plurality of columnar first spacers **(ref. 60)** set up on the first surface of the grid, and a plurality of columnar second spacers **(ref. 56)** set up on the second surface of the grid and abutting against the second substrate; and a voltage supply unit **(ref. 44)**, but fails to teach the voltage supply unit applies a first voltage to the first substrate and applies a second voltage higher than the first voltage to the grid. Compain et al. in the analogous art teaches A voltage supply unit which applies a voltage to the anode and applies a voltage higher than the one for the anode to the grid **(Fig. 5)**. Additionally, Compain teaches incorporation of such a higher voltage to improve the forbidding of generated parasitic ions from reaching the cathode or the anode **(abstract; Fig. 5)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a voltage supply unit which applies a voltage to the first substrate and applies a voltage to the first substrate and applies a

voltage higher than the one for the first substrate to the grid in the image display of Takenaka, since such a modification would improve the forbidding of generated parasitic ions from reaching the cathode or the anode as taught by Compain.

Regarding claim 10, Ge et al. and Compain et al. teach all of the limitations of claim 1, but fail to teach a height correcting layer interposed between the respective first spacers and the first substrate and abutting against the respective first spacers and the first substrate;. Hisafumi in the analogous art teaches a height **(Drawing 3 ref. 15 elastic body)** correcting layer interposed between the respective first spacers **(ref. 14)** and the first substrate **(ref. 11)** and abutting against the respective first spacers and the first substrate. Additionally, Hisafumi et al. teach incorporation of such a height correcting layer to improve the product since the tensile stress value which acts on the front plate, front face and back plate is decreased by 10% and improved breakage prevention is attained **(paragraph 39)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a height correcting layer interposed between the respective first spacers and the first substrate and abutting against the respective first spacers and the first substrate in the spacer of Ge et al. and Compain et al., since such a modification would improve the product since the tensile stress value which acts on the front plate, front face and back plate is decreased by 10% and improved breakage prevention is attained as taught by Hisafumi et al.

Regarding claim 11, Ge, Compain and Hisafumi et al. teach an image display device according to claim 10, wherein each of the first spacers is set up on the first

surface of the grid between the beam passage apertures **(Fig. 1 dotted lines and anode spacer ref. 60).**

Regarding claim 12, Ge, Compain and Hisafumi et al. teach an image display device according to claim 10, wherein the first spacers are shorter than the second spacers in height. The examiner notes that the cathode spacer is 10 to 500 microns. Therefore then choose 510 microns or 501 microns which is 0.51 or 0.501 mm which is about 500 microns. The examiner notes that the anode spacer is about 0.5 mm. Therefore the cathode spacer (second spacer) can be chosen to have greater height than the anode spacer (first spacer).

Regarding claim 16, Compain et al. discloses an image display device according to claim 10, wherein the second voltage applied to the grid is set less than or equal to 1.5 times as high as the first voltage applied to the first substrate **(abstract; Fig. 5)**. This claim is rejected for the same reasons found in claim 1.

Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415, Hisafumi Japanese Patent Application Publication 07-326306, Ge et al. U.S. Patent 5,859,508 and Clifford et al. Japanese Patent Application Publication 10-083778.

Regarding claim 6, Ge, Compain and Hisafumi teach all the limitations of claim 6, but fail to teach the spacers have a high resistance. Ge et al. '508 in the analogous art teaches the spacers have a high resistance **(col. 6 lines 18-21)**. Additionally, Ge et al.

teaches incorporation of such a high resistance spacer to improve the preventing of shorting of the high voltage applied to control the passage of electrons.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a high resistance spacer in the spacers of Ge et al. '771, since such a modification would improve improve the preventing of shorting of the high voltage applied to control the passage of electrons as taught by Ge et al. '508.

Regarding claim 6, Ge, Compain et al. and Hisufami teach all the limitations of the claim, but fail to teach wherein the height correcting layer resistance is low. Clifford in the analogous art teaches wherein the height correcting layer resistance is low **(ref. 112 gold and palladium metal flexible member).** Additionally, Clifford et al. teach incorporation of such a height correcting layer to improve the fixing approach of the spacer in a flat-panel display which can make distribution of a load almost uniform between spacers, and which suits the temperature of a next processing phase, and also suits clarification and the high vacuum environment in a field emission display is demanded **(paragraph 5)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the height correcting layer with resistance low in the display of Ge '771, since such a modification would improve the fixing approach of the spacer in a flat-panel display which can make distribution of a load almost uniform between spacers, and which suits the temperature of a next processing

phase, and also suits clarification and the high vacuum environment in a field emission display is demanded as taught by Clifford et al.

Regarding claim 13, Ge, Compain and Hisafumi teach all the limitations of claim 6, but fail to teach the spacers have a high resistance. Ge et al. '508 in the analogous art teaches the spacers have a high resistance **(col. 6 lines 18-21)**. Additionally, Ge et al. teaches incorporation of such a high resistance spacer to improve the preventing of shorting of the high voltage applied to control the passage of electrons.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a high resistance spacer in the spacers of Ge et al. '771, since such a modification would improve improve the preventing of shorting of the high voltage applied to control the passage of electrons as taught by Ge et al. '508.

Regarding claim 13, Ge, Compain et al. and Hisufami teach all the limitations of the claim, but fail to teach wherein the height correcting layer resistance is low. Clifford in the analogous art teaches wherein the height correcting layer resistance is low **(ref. 112 gold and palladium metal flexible member).** Additionally, Clifford et al. teach incorporation of such a height correcting layer to improve the fixing approach of the spacer in a flat-panel display which can make distribution of a load almost uniform between spacers, and which suits the temperature of a next processing phase, and also suits clarification and the high vacuum environment in a field emission display is demanded **(paragraph 5)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the height correcting layer with resistance low in the display of Ge '771, since such a modification would improve the fixing approach of the spacer in a flat-panel display which can make distribution of a load almost uniform between spacers, and which suits the temperature of a next processing phase, and also suits clarification and the high vacuum environment in a field emission display is demanded as taught by Clifford et al.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415, Hisafumi Japanese Patent Application Publication 07-326306 and Dean U.S. Patent 5,726,529.

Regarding claim 7, Ge, Compain Hisafumi et al. teach all the limitations of the claim, but fails to teach wherein the second spacers have a surface resistance lower than a surface resistance of the first spacer. Dean et al. in the analogous art teaches wherein the second spacers have a surface resistance **(ref. 212 sheet resistance less than 10^{10} ohms/square)** lower than a surface resistance of the first spacer **(ref. 218 sheet resistance greater than 10^{10} ohms/square)**. Additionally, Dean et al. teach incorporation of such a second spacer surface resistance lower than a surface resistance of the first spacer to improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated **(col. 2 lines 12-15)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use wherein the second spacers have a surface resistance lower than a surface resistance of the first spacers in the display of Ge, Compain and Hisafumi et al., since such a modification would improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated as taught by Dean et al.

Regarding claim 14, Ge, Compain Hisafumi et al. teach all the limitations of the claim 14, but fails to teach wherein the second spacers have a surface resistance lower than a surface resistance of the first spacer. Dean et al. in the analogous art teaches wherein the second spacers have a surface resistance **(ref. 212 sheet resistance less than 10^{10} ohms/square)** lower than a surface resistance of the first spacer **(ref. 218 sheet resistance greater than 10^{10} ohms/square)**. Additionally, Dean et al. teach incorporation of such a second spacer surface resistance lower than a surface resistance of the first spacer to improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated **(col. 2 lines 12-15)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use wherein the second spacers have a surface resistance lower than a surface resistance of the first spacers in the display of Ge, Compain and Hisafumi et al., since such a modification would improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated as taught by Dean et al.

Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415, Hisafumi Japanese Patent Application Publication 07-326306 and Ge et al. U.S. Patent 5,859,508.

Regarding claim 8, Ge '771, Compain and Hisafumi teach all the limitations of claim 8, but fail to teach wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment. Ge '508 in the analogous art teaches wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment **(col. 15 lines 65-67;Fig. 6 ref. 524)**. Additionally, Ge '508 teaches incorporation of such a high-resistance surface treatment to improve the prevention of shorting **(col. 6 line 20)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an high-resistance surface treatment of each beam passage aperture in the grid of Ge '771, since such a modification would improve the prevention of shorting as taught by Ge '508.

Regarding claim 15, Ge '771, Compain and Hisafumi teach all the limitations of claim 15, but fail to teach wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment. Ge '508 in the analogous art teaches wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment **(col. 15 lines 65-67;Fig. 6 ref. 524)**. Additionally, Ge '508 teaches incorporation of such a high-resistance surface treatment to improve the prevention of shorting **(col. 6 line 20)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an high-resistance surface treatment of each beam passage aperture in the grid of Ge '771, since such a modification would improve the prevention of shorting as taught by Ge '508.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415 and Dean U.S. Patent 5,726,529.

Regarding claim 17, Ge' 771 teaches an image display device **(title)** comprising: a first substrate **(Fig. 1 anode plate ref. 12)** including an image display surface **(ref. 52)** and a metal back **(ref. 32 Al coating)** formed on the image display surface; a second substrate **(cathode substrate ref. 16) o**pposed to the first substrate across a gap **(Fig. 1 no ref. #)** and including a plurality of electron sources **(FE cathodes ref. 14)** which excite **(ref. 33) the** image display surface; a grid **(ref. 50)** provided between the first and second substrate and including a first surface opposed to the first substrate, a second surface opposed to the second substrate, and a plurality of beam passage apertures **(through hole no ref. #)** opposed to the electron sources, individually; a plurality of spacers **(ref. 60 and ref. 56)** which maintain the space between the first substrate and the second substrate, the spacers including a plurality of columnar first spacers **(ref. 60)** set up on the first surface of the grid and abutting against the first substrate, and a plurality of columnar second spacers **(ref. 56)** set up on the second surface of the grid and abutting against the second substrate, and a voltage supply unit **(ref. 44)**, but fails to teach the voltage supply unit applies a first voltage to the first substrate and applies a

second voltage higher than the first voltage to the grid. Compain et al. in the analogous art teaches a voltage supply unit which applies a voltage to the anode and applies a voltage higher than the one for the anode to the grid **(Fig. 5)**. Additionally, Compain teaches incorporation of such a higher voltage to improve the forbidding of generated parasitic ions from reaching the cathode or the anode **(abstract; Fig. 5)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a voltage supply unit which applies a voltage to the first substrate and applies a voltage to the first substrate and applies a voltage higher than the one for the first substrate to the grid in the image display of Takenaka, since such a modification would improve the forbidding of generated parasitic ions from reaching the cathode or the anode as taught by Compain.

Regarding claim 17, Ge and Compain teach all the limitations of the claim 17, but fail to teach wherein the second spacers have a surface resistance lower than a surface resistance of the first spacer. Dean et al. in the analogous art teaches wherein the second spacers have a surface resistance **(ref. 212 sheet resistance less than 10^{10} ohms/square)** lower than a surface resistance of the first spacer **(ref. 218 sheet resistance greater than 10^{10} ohms/square)**. Additionally, Dean et al. teach incorporation of such a second spacer surface resistance lower than a surface resistance of the first spacer to improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated **(col. 2 lines 12-15)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use wherein the second spacers have a surface resistance lower than a surface resistance of the first spacers in the display of Ge, Compain since such a modification would improve the reducing of electrical charging at its surfaces, which reduces power losses within the display, and which is easily and economically fabricated as taught by Dean et al.

Regarding claim 18, Ge disclose an image display device according to claim 17, wherein each of the first spacers is set up on the first surface of the grid between the beam passage apertures, and each of the second spacers is set up on the second surface of the grid between the beam passage apertures and aligned with the first spacer **(Fig. 1 ref. 60 and 56)**.

Regarding claim 19, Ge disclose an image display device according to claim 17, wherein the first spacers are shorter than the second spacers in height. The examiner notes that the cathode spacer is about 10 to 500 microns. Therefore then choose 510 microns or 501 microns which is 0.51 or 0.501 mm which is about 500 microns. The examiner notes that the anode spacer is about 0.5 mm. Therefore the cathode spacer (second spacer) can be chosen to have greater height than the anode spacer (first spacer).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by Ge et al. U.S. Patent Application Publication 2002/0000771A1 in view of Compain et al. U.S. Patent 6,683,415, Dean U.S. Patent 5,726,529 and Ge et al. U.S. Patent 5,859,508.

Regarding claim 20, Ge '771, Compain and Dean teach all the limitations of claim 15, but fail to teach wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment. Ge '508 in the analogous art teaches wherein a surface of the grid and an inner surface of each beam passage aperture are subjected to high-resistance surface treatment **(col. 15 lines 65-67;Fig. 6 ref. 524)**. Additionally, Ge '508 teaches incorporation of such a high-resistance surface treatment to improve the prevention of shorting **(col. 6 line 20)**.

Consequently it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use an high-resistance surface treatment of each beam passage aperture in the grid of Ge '771, since such a modification would improve the prevention of shorting as taught by Ge '508.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Zimmerman whose telephone number is (571) 272-2466. The examiner can normally be reached on M-W 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn Zimmerman

Vip Patel
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